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REMARKS

Rejection of Claims 1-6 and 8-11.

The Examiner rejected Claims 1-6 and 8-11 under 35 U.S.C. 103(a) as being unpatentable over Pan (U.S. Patent No. 5,595,919) in view of Wu (U.S. Patent No. 6,190,977). The Applicants respectfully traverses the rejection of Claims 1-6 and 8-11. The Examiner stated that Pan discloses the steps of:

providing a gate oxide and gate;

performing a source/drain extension implant (30, fig. 9);

forming spacer on the gate (22, fig. 3);

removing the spacer (fig. 7); and

performing a halo implant (34, fig. 11) (col. 2, ln. 59 - col. 3, ln. 54).

The source/drain extension implant (30) of Pan is a "lightly doped source and drain region 30." The creation of the lightly doped source and drain region 30 is described in column 3, lines 41, 42 and in Figure 9 of Pan. Specifically, in Pan, the lightly doped source and drain region 30 is created *after* removing the spacer, *not before* forming the spacer. Removal of the spacer is described earlier in column 3, lines 34-35, wherein "The silicon nitride walls 22 are stripped."

The Examiner relies upon Wu to teach:

the gate defining a channel region of no more than 50 nm length (col. 1, lns. 54-76);

performing epitaxy to form raised source/drain regions (26, fig. 5); and

forming a silicide (32a,b, fig. 7) on the gate and source/drain regions (col. 5, lns. 50-56 and col. 6, lns.14-37).

However, in col. 1, lns. 54-76, Wu merely describes the need for "shorter channels", and provides no enablement for shorter channels, or dimensions defining what length shorter channels might be. The Applicant respectfully traverses the Examiner's reliance upon Wu to provide 50 nm length channels because Wu fails to provide either enablement or dimensions for short channels.

In contrast to Pan, even in view of Wu, the present method of Claim 1 comprises:

providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

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performing a source/drain extension implant;

forming a spacer on the gate;

performing epitaxy to form raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer;

performing a halo implant; and

completing the MOSFET.

The step of "performing a source/drain extension implant" describes forming the source/drain junctions 11 of the present application. The source/drain junctions 11 are formed before the raised source/drain regions are formed, and as such, the source/drain junctions 11 extend from the isolation trenches 6 to the gate 3, as shown in Figure 1 of the present application. The lightly doped source and drain regions 30 of Pan are formed *after* the oxide layer 26 has been formed, and the spacer 22 has been removed. As a result, the lightly doped source and drain regions 30 extend between the oxide layer 26 and the gate 16 of Pan. Therefore, the Applicant respectfully submits that the lightly doped source and drain regions 30 of Pan are not the source/drain junctions 11 of the present invention, and that the lightly doped source and drain regions 30 of Pan could not be formed by the present method of Claim 1.

Further, Claim 5 of the present application comprises the steps of:

providing a substrate having a gate oxide and gate thereon, the gate defining a channel region of no more than 50 nm length;

performing a vertical source/drain extension implant to a depth of approximately 10 nm to approximately 30 nm;

forming a spacer on the gate;

forming raised source/drain regions;

forming a silicide on the gate and source/drain regions;

removing the spacer;

performing a halo implant; and

completing the MOSFET.

Also, Claim 5 includes the same order of relevant steps that were described in Claim 1, and the same arguments apply. The step of "performing a vertical source/drain extension implant" is performed before "forming a silicide on the gate and source/drain regions." As a result, the source/drain extensions of the present invention extend from the isolation trenches 6 to the gate 3, unlike the lightly doped source and drain regions 30 of Pan which only extend between the oxide layer 26 and the gate 16 of Pan.

In addition, Claim 10 likewise includes the same order of relevant steps that were described in Claim 1, and the same arguments again apply. The step of "performing a vertical source/drain extension implant" is performed before "performing epitaxy to form raised source/drain regions." As a result, the source/drain extensions of the present invention extend from the isolation trenches 6 to the gate 3, unlike the lightly doped source and drain regions 30 of Pan which only extend between the oxide layer 26 and the gate 16 of Pan.

Thus, all the independent claims (i.e., Claims 1, 5, and 10) include a limitation that the source/drain junctions 11 are formed *before* the raised source/drain regions are formed; and, as such, the source/drain junctions 11 extend from the isolation trenches 6 to the gate 3, as shown in Figure 1 of the present application. Consequently, the lightly doped source and drain region 30 of Pan cannot be formed by the method of the present invention.

Rejection of Claim 8.

The Examiner further rejected Claim 8 over Pan, in view of Wu. Based on the above argument, Claim 5 from which Claim 8 depends is not disclosed by Pan, therefore Claim 8 is not disclosed by Pan, even in view of Wu.

The Applicant further points out that the lightly doped region 30 is essential to Pan, even in view of Wu. The first sentence of the abstract of Pan focuses on the LLD structure:

A method for forming an LDD structure using a self-aligned halo process is described

As shown above, the methods of the present invention cannot result in the lightly doped (LLD) regions described in Pan as being the goal of the teachings in Pan.

In the Summary, column 1, lines 45-54, Pan teaches:

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A principal object of the present invention is to provide an effective and very manufacturable method of forming an LDD structure.

A further object of the invention is to provide a method of forming an LDD structure having reduced short channel effects while not increasing junction capacitance.

Yet another object is to provide a method of forming an LDD structure using halos having reduced short channel effects while not increasing junction capacitance.

Thus, Pan clearing points out that the LDD is the essential feature of Pan, and the halo as secondary to the LDD. *There is no mention of the halo independent of the LDD in the summary of Pan.*

Further, Pan describes a halo in a small critical region relative to the LLD in column 1 lines 35 through 38:

It is desirable to provide a process to form a halo only in the small critical region

Comparing Figure 11 of Pan with Figure 5 of the present application, it is clear that the halo of Pan is horizontally limited to the region of the LDD, and the halo of Pan electrically cooperates with the LDD. The halo of the present invention substantially over laps the source drain region 11.

The foregoing discussion establishes first that the methods of the present invention cannot result in the lightly doped source and drain regions 30 (i.e., the LDD) of Pan and that the LDD is an essential element of Pan.

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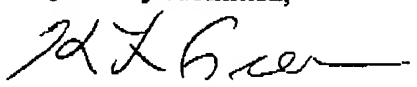
CONCLUSION

Applicant believes that the claims are allowable as originally filed. Applicant respectfully submits that the presently claimed invention is patentably distinct over the cited references; and Applicant therefore believes that the pending claims are non-obvious in view of Pan et al., even in view of Wu, as required by 35 U.S.C. 103. Therefore Applicant believes the present invention is patentable as claimed. In view of the foregoing arguments, favorable consideration by the Examiner, withdrawal of the present rejections, allowance of the pending claims, and passage of the present application to issuance are accordingly solicited. **The Examiner is cordially invited to telephone the undersigned for any reason which would advance the pending claims toward allowance.**

Respectfully submitted,



Kenneth L. Green
Reg. No. 44,724

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LaRIVIERE, GRUBMAN & PAYNE, LLP
Post Office Box 3140
Monterey, CA 93942
(831) 649-8800